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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/761,497	01/16/2001	Eugene A. Fitzgerald	Amber.5342B	5902

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EXAMINER	
NGUYEN, THINH T	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/761,497	FITZGERALD, EUGENE A.	
	Examiner	Art Unit	
	Thinh T Nguyen	2818	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED OFFICE ACTION

Specification

1. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

2. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,2,3,4,5,6,7, 8,9,10,11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jewell (U.S. patent 5859864) in view of Bensahel et al. (U.S. patent 6117750), Brasen et al. (US patent 5442205) and in view of further remark.

REGARDING TO CLAIM 1

Jewell discloses in his invention a method for processing a semiconductor structure comprising:

A substrate (fig 2a and column 12 line 40-41); a lattice-mismatched first layer (fig 2a layer 28) deposited on the substrate and; and a second layer deposited on the first layer (fig 2a layer 30) with a greater lattice mismatch to the substrate than the first layer.

Although Jewell do not use annealing method for lower the threading dislocations, Bensahel et al. refer in (column 1 line 64-67 and column 2 line 1-6) the use of annealing after deposition of the GeSi layer on top of the substrate layer to reduce the threading dislocation from lattice mismatch of the two layers.

It would have been obvious to one have ordinary skill in the art at the time the invention was made to use the teachings of Jewell and Bensahel and his ordinary skill in order to produce a semiconductor device with low dislocation densities by annealing at a temperature greater than 100 degree C above the deposition temperature of the upper layer since it has been held that where the general condition of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art.

In re Aller, 105 USPQ 233.

The reasoning is as follows:

A person of ordinary skill in the art would have been motivate to perform the annealing As taught by Bensahel on the process invented by Jewell in order to formulate a method of fabrication of a semiconductor device that have low threading dislocation density.

REGARDING TO CLAIM 2

Brazen et al. in (fig 2) shows a method to make a semiconductor structure of a silicon substrate (fig 2 Layer 1) with the first (fig 2 layer 2) and second layer (fig 2 layer 3) that are made of $Si_{1-x}Ge_x$.

REGARDING TO CLAIM 3

Jewell shows a method to make a semiconductor structure (column 3 line 6-10 and fig 2a) with a GaAs substrate, and the first and second layers made of $In_y Ga_{1-y} As$.

REGARDING TO CLAIM 4

Jewell shows a method to make a semiconductor structure (column 3 line 6-10 and fig 2a) with a GaP substrate and the first and second layers made of $In_z Ga_{1-z} P$.

REGARDING TO CLAIM 5 AND 6

The selection of the percent of Ge concentration to achieve needed results in the process of making semiconductor is considered a routine ordinary skill.

It would have been obvious to one having ordinary skill in the art at the time the Invention was made to select the right concentration for Germanium since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215

REGARDING TO CLAIM 7,8, 9, 10, AND 11

The selection of the growth temperature , the annealing temperature and the annealing time to achieve needed results in the process of making a semiconductor is considered of routine ordinary skill.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to select the right growth temperature ,the right annealing temperature and the right annealing time since it has been held that discovering an optimum value of a resulted effective variable involves only routine skill in the art.

In re Boesch, 617 F.2d 272, 205 USPQ 215

REGARDING TO CLAIM 12

Bensahel et al. (in the abstract) teach the use of chemical vapor deposition method to deposit the lattice-mismatched semiconductor layer.

4. Claims 13,14, 15, 16,17,18,19,20,21,22,23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jewell (U.S. patent 5859864) in view of Bensahel et al.(U.S. patent 6117750), Brasen et al. (US patent 5442205) and in view of further remark.

REGARDING TO CLAIM 13

Jewell discloses in his invention a method for making a semiconductor structure comprising: a substrate(fig 2a and column 12 line 40-41); a lattice-mismatched first layer (fig 2a layer 28)deposited on the substrate and; and a second layer deposited on the first layer (fig 2a layer 30) with a greater lattice mismatch to the substrate than the first layer.

Although Jewell do not use annealing method for lower the threading dislocations, Bensahel et al. refer in (column 1 line 64-67 and column 2 line 1-6) the use of annealing after deposition of the GeSi layer on top of the substrate layer to reduce the threading dislocation from lattice mismatch of the two layers.

It would have been obvious to one have ordinary skill in the art at the time the invention was made to use the teachings of Jewell and Bensahel et al. and his ordinary skill in order to produce a semiconductor device with low dislocation densities by annealing at a temperature greater than 100 degree C above the deposition temperature of the upper layer since it has been held that where the general condition of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art.

in re Aller, 105 USPQ 233.

The reasoning is as follows:

A person of ordinary skill in the art would have been motivate to perform the annealing As taught by Bensahel on the process invented Jewell in order to formulate a method of fabrication of a semiconductor device that have low threading dislocation density.

REGARDING TO CLAIM 14

Brasen et al. (fig 2) show a method for making a semiconductor structure of a silicon substrate (fig 2 Layer 1) with the first (fig 2 layer 2) and second layer (fig 2 layer 3) that are made of $Si_{1-x}Ge_x$.

REGARDING TO CLAIM 15

Jewell shows a method for making a semiconductor structure (column 3 line 6-10 and fig 2a) with a GaAs substrate, and the first and second layers made of $In_yGa_{1-y}As$.

REGARDING TO CLAIM 16

Jewell shows a method for making a semiconductor structure (column 3 line 6-10 and fig 2a) with a GaP substrate and the first and second layers made of $In_zGa_{1-z}P$.

REGARDING TO CLAIM 17 AND 18

The selection of the percent of Ge concentration to achieve needed results in the process of making semiconductor is considered a routine ordinary skill.

It would have been obvious to one having ordinary skill in the art at the time the Invention was made to select the right concentration for Germanium since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215

REGARDING TO CLAIM 19,20,21,22, AND 23

The selection of the growth temperature, the annealing temperature and the annealing time to achieve needed results in the process of making a semiconductor is considered of routine ordinary skill.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to select the right growth temperature ,the right annealing temperature and the right annealing time since it has been held that discovering an optimum value of a resulted effective variable involves only routine skill in the art.

In re Boesch, 617 F.2d 272, 205 USPQ 215

REGARDING TO CLAIM 24

Bensahel et al. (in the abstract) teach the use of chemical vapor deposition to deposit the lattice-mismatched semiconductor layer.

5. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

6. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

CONCLUSION

7. The prior arts made of record and not relied upon are considered pertinent to applicant disclosure: Calviello et al.(US patent 5159413)disclose a monolithic integrated circuit having compound semiconductor epitaxially grown on ceramic substrate, Inoue (US patent 5252173) reveal a process for growing semiconductor layer on substrate, Tuppen et al.(US patent 5279687) disclose a method for preparing substrate by annealing epitaxial layer in the form of mesa and substrate SO prepared, Karam et Al. (US patent 6010937) teach the reduction of dislocation in a heteroepitaxial semiconductor structure, Mishima et al. (US patent 5633516)show a lattice-mismatched crystal structures and semiconductor using the same.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose phone number is (703) 305-0421. The Examiner can normally be reached on Monday to Friday from 8.30 A.M. to 5.00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, David C. Nelms can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Thinh T. Nguyen TTN

Art Unit 2818